FACULTY PROFILE

Dr. Nanduri Samba Murthy

S.R. Gudlavalleru Engineering College
Phone No: 08674 – 273737, 273888 (O)

Career Objective:

Aim to be associated with a progressive organization that gives me scope to update my knowledge and skills in accordance with latest trends and be a part of team to work in seeking to be a professional in the field of Electronics and Communication working in a good organization that to the growth of the organization.

Academic Qualifications

S. No	Name of the Degree *(Starting from Ph.D to 10th Class)*	University/College	Percentage of Marks/Grade	Specialization
1.	Ph.D	JNTUK, KAKINADA	2024	Low Power Embedded system Design
2.	M.TECH	GUDLVALLERU ENGG.COLLEGE, GUDLAVALLERU	79.5%	Embedded systems
3.	B.TECH	JNTUH, HYDERABAD.	61.85	ECE
4.	DIPLOMA	A.A.N.M&V.V.R.S.R POLYTECHNIC, GUDLAVALLERU	71.40%	ECE
5.	S.S.C	P.L.S. Z.P.HIGH SCHOOL,AKIVIDU	76.5%	Telugu&Sanskrit

Professional Experience

S. No	Designation	Institution Name	Working Period	
			From	To
1.	Lecturer	A.AN.M&VVRSR POLYTECHNIC Gudlavalleru.	2008	2013
2.	Assistant Professor	GUDLAVALLERU ENGG.COLLEGE	2013	Till Date

Professional Body Membership

S. No	Name of the Professional body	Membership Number
1.	The Institute of Engineers (India)	AM157511-5
2.	Institute of researchers	LM012203

Papers Published in Reputed Journals No. : 10

1. N.Sambamurthy and M.Kamaraju, "FPGA implementation of high performance image de-noising filter," Analog Integrated Circuits Signal Processing, vol.118, issue-3, pp. 387–398, 2024. **(SCI Indexed)**

2. N.Sambamurthy and M.Kamaraju, "Scalable intelligent median filter core with adaptive impulse detector," Analog Integrated Circuits Signal Processing, vol.118, issue-4, pp. 425–435, 2024. **(SCI Indexed)**

SCOPUS Indexed: 06

3. Sambamurthy, N., Kamaraju, M. Reconfigurable AI-enabled vectored median filter for real-time image denoising and edge preservation in FPGA-based smart imaging systems. Multimed. Tools and Appl. **(2025)**. https://doi.org/10.1007/s11042-025-20664-x

4. N.Sambamurthy, M.Kamaraju, "Energy-Efficient Median Filter Core Architecture for Impulse Noise Removal in Smart Measurement Systems," SN COMPUT.SCI. vol.5, issue-1, pp.154-162, 2024. (Scopus Indexed)

5. N.Sambamurthy, M.Kamaraju,"FPGA Based Optimized Reconfigurable Base-2 Constant Coefficient Multiplier Architecture for Image Filtering," International Journal of Engineering and Advanced Technology (IJEAT), vol.9, issue-4, pp.822-825, 2019. (Scopus Indexed)

6. N.Sambamurthy, M.Kamaraju, "FPGA implementation of PSO Based RGB-Y Filter," International Journal of Advanced Trends in Computer Science and Engineering, vol.9, issue-4, pp.5003-5008, 2020. (Scopus Indexed)

7. N.Sambamurthy, M.Kamaraju, "FPGA based computational efficient and low power median filter," Journal of critical reviews, ISSN-2394-5125, vol.7, issue-19, pp.8879-8893, 2020. (Scopus Indexed)

8. N.Sambamurthy, M.Kamaraju, "Area and Power efficient Comparator and swap switching network for Median filter", Journal of solid technology, vol.63, issue-6, pp.17217-17227, 2020. (Scopus Indexed)

UGC Care: 01

9. N.Sambamurthy, M.Kamaraju, "Power optimised hybrid sorting-based median filtering," International Journal of Digital Signals and Smart Systems, vol.4, issue-3, pp.80-86, 2019.

International Conference (Springer):01

10. N.Sambamurthy, M.Kamaraju, “High-Performance Image Visual Feature Detection and Matching”, Advances in Communications, Signal Processing, and VLSI, Lecture Notes in Electrical Engineering, vol.722, Springer, Singapore, pp.249-261, 2021. (Scopus Indexed)

Patent Grant : 01

11. A patent has been granted to M.Kamaraju and Nanduri Sambamurthy for their invention titled **"Efficient Embedded Programmable Architecture Design of Multi-Channel and Multi-Kernel Supported Vectored Median Filter System"**. The patent, with grant number **554936**, was granted on **November 25, 2024**.

Papers Published in National Conferences No. : 01

12. M. Kamaraju, N.Sambamurthy, “FPGA Implementation of Multiprocessor Core Architecture with Multichannel UART” NCIET-2014, PP. 265-269.

Certifications/short term Programs Attended in premier institutes No. 05

1. 15 days orientation program on “Research Methodology”, organized by JNTUK, KAKINADA during 1st - 15th May 2015.
2. 15 days orientation program on “Intellectual property rights”, organized by JNTUK, KAKINADA during 16th-30th May 2015.
3. Faculty Development Program on “VLSI and Embedded System Design” organized by department of ECE, Gudlavalleru Engineering College, Gudlavalleru during 7th – 8th July 2012.
4. Faculty Development Program on “VLSI Architectures for Energy efficient Embedded health care systems” from **26th to 28th February 2021**, organized by school of Electrical sciences, **IIT Bhubaneswar, Odisha**.
5. Faculty Development Program on SPARC sponsored Indo-USA online short term course on signal processing and machine learning techniques for **data driven IoT and smart phone health monitoring held from 26-30 March,2021** organized by school of electrical sciences, **Indian Institute of Technology, Bhubaneswar, odisha.**

Guest Lectures Delivered No. : 03

1) "Concurrent computing", for faculty at Gudlavalleru Engineering College, Gudlavalleru on 9th April 2014.

2) "Low power VLSI techniques", for faculty at Gudlavalleru Engineering College, Gudlavalleru on 27th septemer2016.

3) "An overview on python programming and its use in hardware Design", acting as resource person(29-6-21,10:00A.M-12:00PM(IST), for AICTE sponsored short term Training program on FPGA based digital system design with HDL. 28th july-July 03rd,2021. VEL tech Multitech Dr.Rangarajan, Dr.Sakunthala Engineering college, Tamilnadu, affiliated to Anna university.

Workshops /Conferences /Seminars Attended No. : 09

1. One day seminar on "Engineering education and research" conducted by NI instruments, 19th July 2015.

2. One week workshop on "Advances in VLSI design" conducted by IIT Kharagpur during 2nd -6th January 2015.

3. One day workshop on "Research in Energy Management Wireless Networks & Smart Transportation Systems" organized by The Institute of Engineers (India), Vijayawada Local Centre, Vijayawada on 29th March 2015.

4. One day workshop on "Research & Development Facilitation" organized by The Institute of Engineers (India), Vijayawada Local Centre, Vijayawada on 29th March 2015.

5. One day workshop on "Speech Processing: Current Challenges and Hands-on Experience" organized by department of ECE, Gudlavalleru Engineering College, Gudlavalleru on 23rd August 2014.

6. Three day National Workshop on "Theory & Applications of Intelligent Signal Processing", organized by department of ECE, Gudlavalleru Engineering College, Gudlavalleru during 28th February to 2nd March 2014.

7. Two week ISTE workshop on "Signals & Systems" conducted by IIT Kharagpur in association with department of ECE, Gudlavalleru Engineering College, Gudlavalleru during 2nd -12th January 2014.
8. Two day FDP on VLsi architectures for embedded health care systems 26th -28th February 2021,IIT Bhubaneswar,2021.

9. Signal processing and Machine learning techniques for data driven Iot techniques for smart phone and health monitoring.26th -30th, 2021, IIT Bhubaneswar .

Subjects Handled

Under Graduation: 14

1. Electronics measurements and instrumentation
2. Microprocessor and microcontrollers
3. Computer Networks
4. Microprocessors and Multicore systems
5. Microprocessors and Micro controllers Applications
6. Embedded system Design
7. Introduction to Internet of Things.
8. Electronics measurements and instrumentation principles.
9. TRENDS in IoT
10. CMOS VLSI Design
11. Embedded system based IoT
12. Digital Image Processing
13. Principles of VLSI Design
14. Linear and Digital IC Applications

Post-Graduation:10

1. Embedded system design
2. Sensors and actuators
3. Soc design
4. Parallel processing
5. Embedded systems lab
6. Low power VLSI design

Laboratories Handled

Under Graduation: 5

1. Microprocessor and microcontrollers Lab
2. Microprocessors and interfacing Lab
3. IoT Lab
4. Basic electronics lab
5. LICA LAB
6. Data structures using python lab

Post Graduation: 4

1. Embedded systems lab
2. HDL Simulation lab
3. IoT Lab
4. CMOS design LAB
5. HDL Simulation lab
6. CMOS VLSI design Lab
7. IoT LAB
8. Advanced Microcontrollers LAB
9. Data structures using Python programming

Other Responsibilities

College Level:

1. Disciplinary committee at the time of GEC FEST-2013, 2014,2015,2016,2017.
2. Unnat Bharat Abhiyan Programme co-coordinator.
3. SoP Member during Covid -19
4. NAAC -7 criteria incharge/community engagement
5. Community Service Project Coordinator/Master of Trainer

Department Level:

1. Internal examinations co-ordinator for the year 2014-2017.
2. IETE Faculty advisor.
3. Internship coordinator.
4. Industrial Supported IoT Lab In- charge 2019-2021.
5. ATAL Coordinator
6. Class teacher during 2015-2025
7. GENECES-2021 Coordinator.

Extra Curricular Activities:

1. Acted as BoS member for department of ECE, Gudlavalleru Engineering College, Gudlavalleru on 2nd August 2014, 25th May 2015 and 1st March 2017 and 2022.

Projects Guided: Under Graduation

S. No	Name of the project	Year
1.	FPGA implementation of automatic tollgate systems	2013
2.	Microcontroller based traffic guidance system	2014
3.	FPGA implementation of number plate recognition	2015
4.	PC Based Two Channel Oscilloscope	2016
5	FPGA implementation of low power RISC Processor	2017
6.	FPGA implementation of self timed adder	2018
7.	FPGA implementation of low power Median filter	2019
8.	FPGA implementation of low power 2D wavelet based Multiplier.	2020
9.	DWT based MAC	2021
10.	FUSED then add Multiplier	2022
11	Power optimized MAC	2023
12	FPGA based object detection	2024

Post Graduation:

S.No	Name of the project	Year
1.	Prevention of train accidents using wireless sensor networks	2013
2.	Design and analysis of AES encryption and decryption	2014
3.	Power optimized CODEC	2015
4.	Design and analysis of logic-in-memory based multiprocessor architecture for multi data transfer schemes	2016

Academic Rewards / Achievements:

1. **Class Topper in M.TECH Embedded system in SRGEC, Gudlavalleru.**
2. First Prize in startup Idea innovation at all India level sponsored by Department of science and technology. Nectar, North india,
3. Young Researcher award from Institute of Researchers on 2021, in recognition of professional and research achievements.
4. **Act as reviewer of SCI and Scopus Journals From 2021-2025.**
    1. Measurement Scopus and SCi journals
    2. Image Signal Video Processing --- SCi journals
    3. Multimedia systems--- SCi journals
    4. Journal of Bionic engineering--- SCi journals
    5. New Generation Computing---- SCi journals

Books Published No. : 02

1. **N.SAMBAMURTHY,** Titled by **"COMMUNICATION ENGINEERING",** For Polytechnic ECE Students Published by FALCON publishers, Hyderabad, 2012.

2. **N.SAMBAMURTHY,** Titled by **"PYTHON PROGRAMMING WITH REAL-TIME APPLICATIONS",** For Diploma, UG, PG Students Published by IIP publishers, Cochin, 2023.

3. **N.SAMBAMURTHY,** Titled by **"Internet of Things Design",** For Diploma, UG, PG Students (In press).

R&D and Consultancy:

S. No	Project Title	Source of Funding	Duration	Role	Status
1.	Real-time hardware based video surveillance for public safety	SRGEC Gudlavalleru	1.5 years	Principal investigator	**On-going**
2.	A Novel Digital auto starter and timer using IoT	MHRD Govt.of India, IIT Delhi.	1 year	Principal investigator	**On-going**
3.	Design and implementation of traffic guidance system	SRGEC Gudlavalleru	1 year, Rs.70,000\-	Co investigator	Completed

Signature of Candidate